MICRO COMPUTER-BASED SOLAR CELL DATA ACQUISITION SYSTEM

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In Partial Fulfilment of the Requirements
for the Degree of
MASTER OF TECHNOLOGY

by

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to the

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CERTIFICATE

Certified that the work entitled 'MICROCOMPUTER-BASED SOLAR CELL DATA ACQUISITION SYSTEM' by Mr. G. Aravanan, has been carried out u nder my supervision and the work has not been submitted elsewhere for a degree.

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ACKNOWLEDGEMENT

It is a pleasure to record my thanks and appreciation for Dr. Hasan's friendly guidance and for the many illuminating discussions I had with him at various stages of this project.

I must also express my appreciation of the co-operative of the ACES Staff, which made the going smooth.

The final form this work took is not a little due to the thought-provoking over-a-cup-of-tea discussions I had with Mr. Ramana, Flt.Lt. Ramanujam and T.V. Prabhakar. Let them be assured of my pleasant memories of our association.

If you find decent drawings in this report, don't put it down to me: I have'somu'to thank for them. Thanks too, to Mr. C.M. Abraham for efficient typing.

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ABSTRACT

The current-voltage (I-V) characteristics of a solar cell completely characterize its performance. Hence the evaluation of the performance of a solar cell requires accurate measurement of its I-V characteristics. Conventional X-Y plotter technique requires further data reduction from the curve, which makes it inconvenient with regard to accuracy and speed. From the above points of view an automated data acquisition and test system for solar cells is highly desirable.

The system described here is built around and INTEL 8080 microprocessor-based microcomputer (MICRO-78 made by Electronics Corporation of India Ltd.). The hardware is composed of a 12 bit D/A converter, a 12 bit A/D converter, a driver, and a sensor circuit interfaced with the microcomputer through programmable peripheral Interface (PPI) cards. The system is made totally modular (both hardware and software wise) to facilitate any further modification. Further, the software and hardware are designed in such a way as to provide automatic gain settings to cater for a variety of solar cells and other semiconductor devices. The same system can be used without modifications, as an I-V data acquisition system for any two terminal device.

CHAPTER 1

INTRODUCTION

Progress in analog instrumentation has been rapid since the introduction of the monolothic operational amplifier in 1965. Recent emphasis on microprocessor and minicomputer applications involving data acquisition, instrumentation and process control has made significant intrusion into the analog world. The movement from small scale integration (SSI) through Medium Scale Integration (MSI) to Large Scale Integration (LSI) and particularly the microprocessor has removed much of the economic advantages of analog instruments. 'Intelligent Instruments' can be built around a microprocessor with the flexibility improving the functional capabilities by software modifications which are easy to implement[1].

1.1 AIM OF THE PROJECT

The aim of the project is to provide a microcomputer-based, modular, solar cell I-V (current-voltage) data acquisition system compatible with a class of microprocessors available in the microprocessor laboratory of IIT Kanpur which could serve as a starting point in the computerization of solid state device data acquisition systems.

The electrical behaviour of a solar cell is completely characterised by its current versus voltage (I-V) curve under

illumination. To obtain this curve, the voltage across the solar cell may be continuously or discretely varied and the corresponding voltage and current variations plotted on an X-Y plotter. However, accuracy, speed, and convenience requirements make it highly desirable to have an automated I-V measurement system. If the measured I-V characteristics can be accurately modelled by a functional relationship such as $I = f(V, I, \lambda_1, \lambda_2 \ldots\ldots \text{etc.})$ where λ_i are appropriate electrical parameters, then, in principle, the λ_i can be evaluated by fitting the mathematical function to the measured I-V curve using

$$I = I_L - I_{o1}\left[\exp\left[\frac{q(V+IR_S)}{A_1 kT}\right] - 1\right] - I_{o2}\left[\exp\left[\frac{q(V+IR_S)}{A_2 kT}\right] - 1\right] - \frac{V}{R_{Sh}} \qquad (1)$$

where,

I → current flowing out of the anode of the solar cell terminals

V → Anode to cathode voltage drop across the solar cell

I_L → Light-generated current

I_{o1} → Dark saturation current due to diffusion

I_{o2} → Dark saturation current due to recombination in the space charge region

A_1, A_2 → 'non-ideality' factors

R_S → Series resistance, and

R_{Sh} → Shunt resistance

Strictly speaking, R_S is a function of the current and equation (1) should be fitted to the experimental I-V curve over only a small region.

The common method of obtaining the experimental illuminated I-V characteristics is by varying an externally applied voltage across the solar cell between zero and its open circuit value and plotting the current and voltage on an X-Y plotter. Several points are read-off the plotted curve and used in a non-linear curve fitting program to find the values of the electrical parameters.

As can be seen, equation (1) is highly nonlinear. Even worse, the values of the different parameters vary over several orders of magnitude. Hence, the experimental data to which equation (1) provides a fit must be measured with a very high degree of accuracy to give any meaningful result. Such accuracy is not possible with the method of reading points off a curve plotted on a graph paper. Besides, a significant amount of labour is involved in reading 20 to 30 points off a plotted curve. With a large number of test points involved, the data reduction time would be inordinately large compared to the data acquisition time. Hence, it is desirable to build a microprocessor-based data acquisition system which, on command applies a large number of voltages across the test solar cell and digitally measures, stores and outputs the voltage and current

values at each data point[2,3]. Since the instrument is microprocessor-based, intelligence can be built-in through software to average a number of data points, skipping insensitive regions and taking more readings in the sensitive regions (e.g. near the open circuit voltage of the solar cell). Further, the microprocessor's calculating power can be used to make other computations (power at each data point, maximum power, fill factor, efficiency etc.).

1.2 SYSTEM CAPABILITIES

The system built provides the following facilities at present :

1. I-V data acquisition of the solar cell under illumination
2. Averaging of data points
3. Software gain control for voltage and current in order to cater for a variety of solar cells, and,
4. Capability of detecting the sensitive regions and accessing data points in such a way as to weight these regions relative to the insensitive regions of the I-V characteristics.

With a single instruction modification and no hardware modification the same system can be used for

1. I-V data acquisition of solar cell under dark
2. I-V data acquisition for any two terminal device with the other facilities remaining the same.

The whole system is made modular both hardware and software-wise to permit facile future modification as required. The hardware interface to the microcomputer is also made programmable to enable hardware modifications.

1.3 OVERVIEW

Chapter 2 deals with the basic system organisation at block-level and describes the function of each block.

The hardware and software elaboration of the system design is dealt with in Chapter 3.

The I-V data of a solar cell, obtained under different illuminations (including the dark I-V) using the system designed and constructed by the author are presented in Chapter 4. The forward-bias I-V characteristic of a diode have also been obtained on this set-up, for test purposes.

In Chapter 5, we present suggestions for modifications of the present system in order to make it more versatile.

CHAPTER 2

BASIC SYSTEM ORGANIZATION

The basic system block diagram is given in Fig. 2.1.

The scheme is as follows :

The microcomputer applies a voltage across the cell through Digital-to-Analog Converter (DAC) and Driver. The resulting current of the device is converted into voltage through the Sensor and is read into the microcomputer via the Analog-to-Digital Converter (ADC) and Sample-Hold circuits. The microcomputer computes the next voltage to be applied and outputs the corresponding digital value into the DAC. The current is again measured in voltage form through the sensor and ADC. This sequence is done from 0 volts to the open circuit voltage of the solar cell (i.e., till the current becomes zero). At each voltage value current is averaged and printed in scaled form.

In designing the hardware system blocks and linking, software control and system flexibility for future modifications are taken into account. The choice of system blocks is a critical factor in building power and flexibility into the system.

2.1 CHOICE OF MICROPROCESSOR/COMPUTER

The normal factors involved in the choice of the processor/system are,

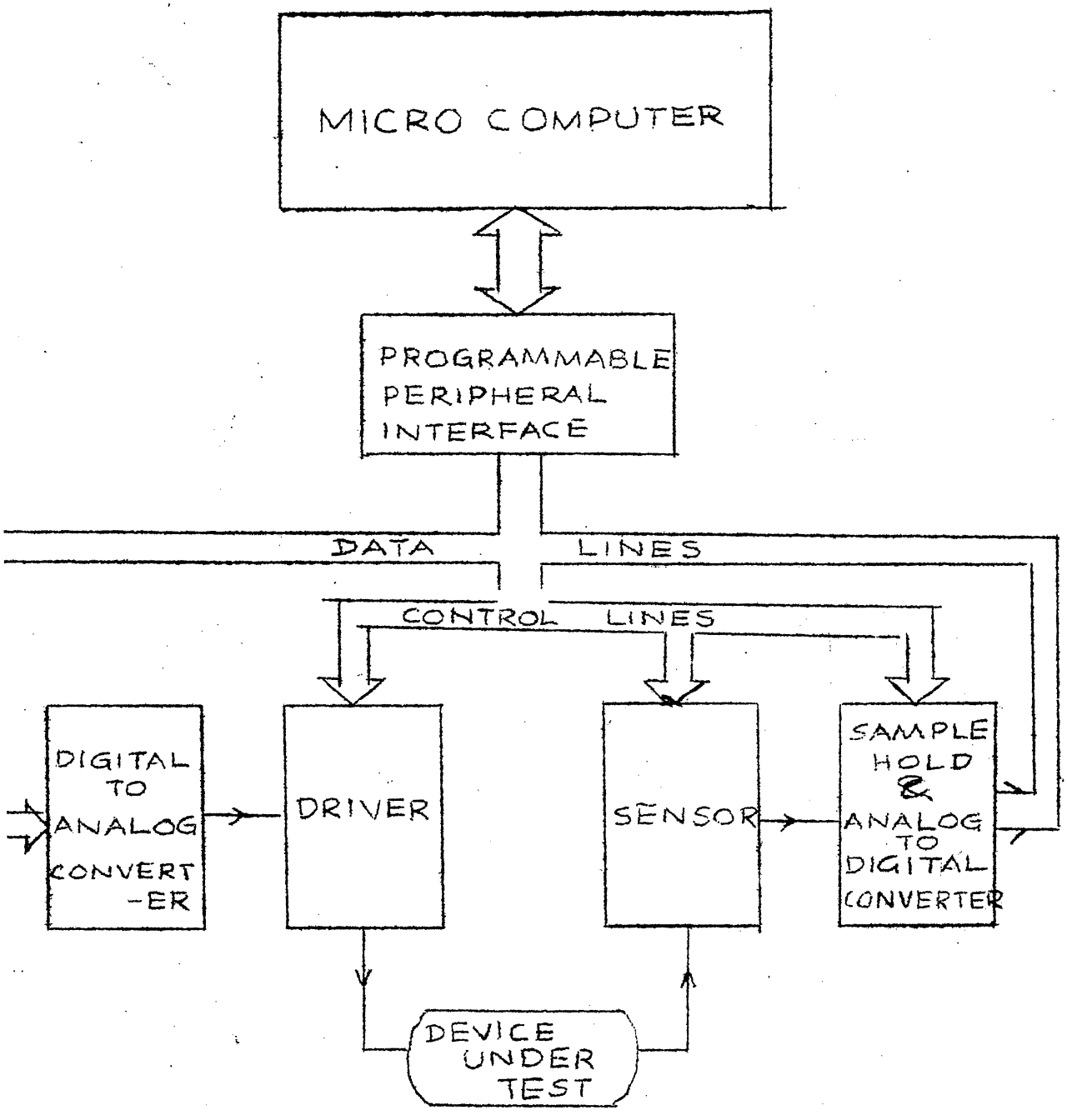


FIG 2·1: BASIC SYSTEM BLOCK DIAGRAM

1) Speed (2) versatility and power of instruction set
3) Word length (4) compatability and ease of interfacing
5) System support, ease of use, and availability in the microprocessor lab.

All these factors are considered along with the nature of application before arriving at a conclusion on system selection.

Our application requires only moderate speed; however the demand on a powerful system with flexibility arises in order to make a general purpose-easy to use instrument. Of the available microcomputers (INTEL 8080 based systems, AMI 6800 system, F8 based system etc.) in the Microprocessor Laboratory, INTEL 8080 microprocessor-based system is the most powerful for it has the maximum hardware and software support. At present, there are four INTEL 8080 microprocessor-based microcomputers (EC MICRO-78) available in the laboratory. The peripheral support includes slow speed tele-types, floppy disc and digital cassette back-up and alpha-numeric display terminals. These systems are made and marketed by ECIL Hyderabad. The system software support includes a resident assembler, On-line Debug System (ODS), BASIC language and a Decimal Arithmetic Package (DAP). Hence the instrument built around MICRO-78 has access to a full fledged microcomputer.

MICRO-78 is an 8-bit parallel microcomputer having the instruction set of INTEL 8080. It has 16-bit direct addressing

capability and has a separate 8-bit I/O address space. In order to interface the instrument to the microcomputer two programmable Interface Cards (PPI's) are made. Each card has three I/O ports and the status of a particular port (in INPUT MODE OR OUTPUT MODE) is software programmable. This flexibility allows for instrument modification with ease and enhances the power of the system. More details of the microcomputer and PPI can be found in the subsequent chapters and Appendix.

2.2 DESIGN CRITERIA

The following design criteria were considered in the basic design.

. The design should allow for sufficient scope for expansion at a later stage depending on the application.

. It should allow changes in the input and output configurations making the system more versatile.

To satisfy these, the design was centered around the following :

2.2.1 Functional Design

1. The entire hardware is divided into functional modules each on separate printed circuit board (for e.g. Digital to Analog Converter and Driver, Sensor, Sample-Hold and Analog to Digital Converter etc.)

2. As explained earlier, the interfaces are made programmable to incorporate changes in the system. Besides the I/O ports used, additionally one I/O port is made available to facilitate the suggested improvements.
3. Software is made modular and new subroutine introduction and linking is easy.
4. The gains of Driver and Sensor are software selectable through user communication command via Tele-type.

Hence any additional functional block such as another DAC or ADC or counter etc., can be introduced along with software without any difficulty.

2.2.2 Mechanical Design

Each functional module is made on a separate printed circuit card of size 20 cms by 10 cms. This card size allows sufficient complexity of circuits to be implemented with the available MSI chips.

Each card is enclosed in a bin made of 3/8" thick aluminium sheet reducing the effects of noise on the circuits. Three different widths of bins 1.35", 2.7" and 4" are used depending upon the size of the external connector in the rear panel and connections brought out on to the front panel. All these modules go into a 5.2" height frame which can be adopted for rack mounting. This scheme paves the way, for integrating

different modules of various sizes depending on the application and at the same time allows rack mounting.

To allow for this small size modules Amphenol 15 pin contact and 25 pin contact miniaturized connectors[4] are used depending on the number of external connections. Space is provided in the main frame to accommodate a few more modules.

Thus the functional design and mechanical design are expected to completely meet the requirements mentioned in the Design Criteria.

2.3 COMPONENT SELECTION AND DESIGN FEATURES

Other than the microcomputer and the interface cards the major functional blocks are (i) Digital to Analog-Converter (ii) Driver, (iii) Sensor and (iv) Sample-Hold and Analog to Digital-Converter circuit. Even though speed is not a major criterion, high accuracy is required to get meaningful data. Hence 12-bit converters are chosen for this purpose. Although the ADC available to us was an inherently slow device and acts as the speed-limiter in the measurements, we decided to use a fast settling, high slew rate buffer as our driver, in order to achieve a modular design which can retain the speed of the DAC. All circuit components are chosen keeping in view ofthe offset, drift, slew-rate etc., in order to retain the system accuracy on all levels. Hence the Driver buffer, Sensor circuit and Sample-H Hold circuit buffer op-amps are chosen with low off-set and

drift. A further requirement for the Sensor and Sample-Hold circuits is low-input bias current. The ADC is a slow-speed monolithic CMOS 12-bit converter working on 'charge-balancing' principle. The Driver and Sensor circuits are made with necessary hardware to provide software gain control. Full details of the circuit diagrams and component descriptions are given in the next chapter.

CHAPTER 3

HARDWARE AND SOFTWARE ORGANIZATION

As pointed out in the earlier chapters, the hardware and software organization should meet the requirements of accuracy and flexibility. Fig. 3.1 shows the microcomputer functional blocks along with the interfaces.

3.1 DESCRIPTION OF MICRO-78[7]

The microcomputer is a small, compact inexpensive 8-bit computer designed to meet the requirements of a variety of applications. The system is built around the LSI, N-channel, Si-gate, MOS single chip processor (INTEL 8080A). This chip interfaces with memory and INPUT/OUTPUT through an 8-line data bus and a 16-line address bus.

The microcomputer has an 8-bit Data word length and a Multiple word instruction format. It has a machine cycle time of 2 microseconds and can directly address upto 64 K bytes of core memory or any standard combination of semiconductor RAM/ROM. It can have 256 input ports and 256 output ports for communication with the external world.

The standard system software includes a basic Assembler, an On-line Debugging System (ODS), a variety of utility packages and mathematical routines and basic hardware diagnostics.

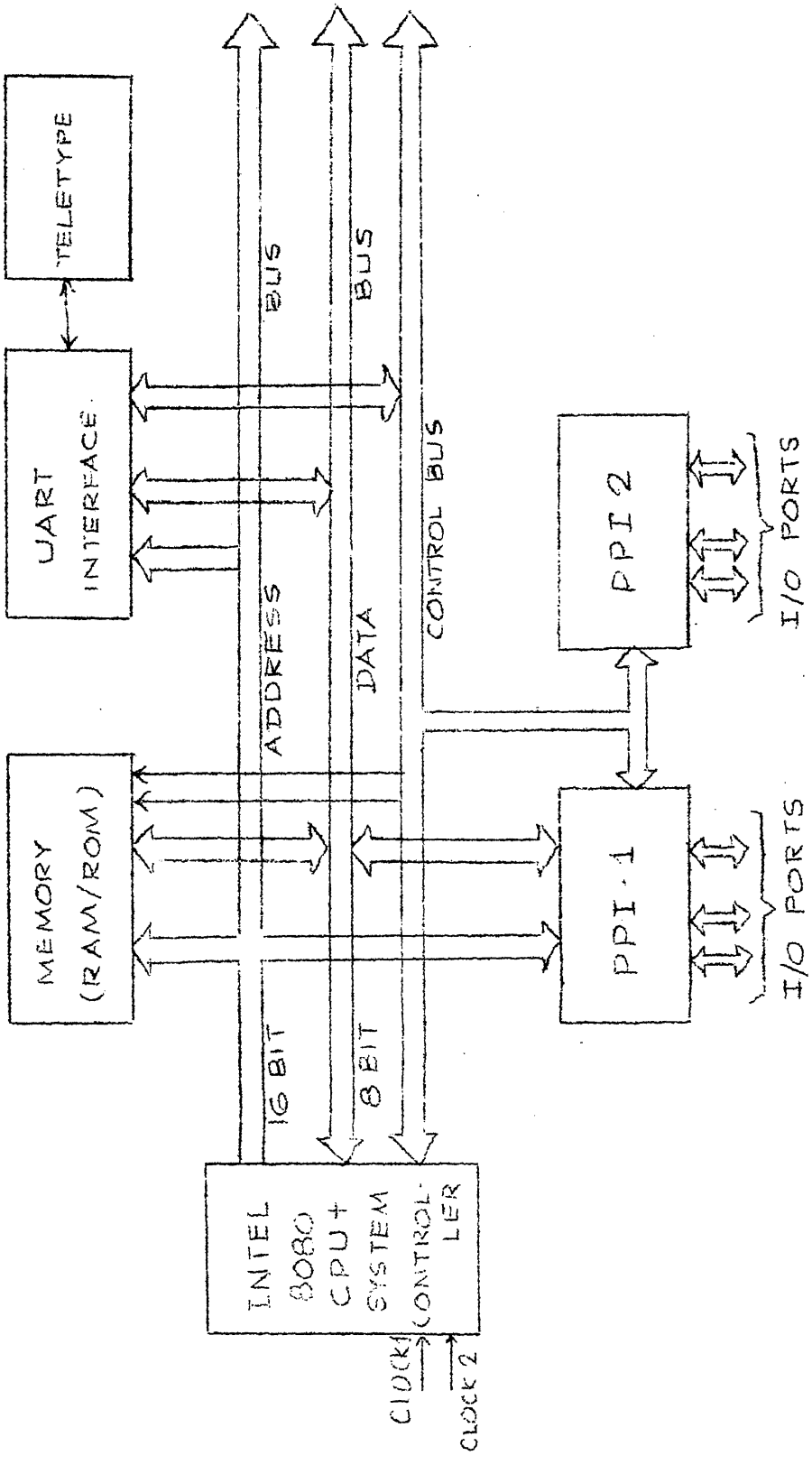


FIG 3.1: MICRO-78 AND INTERFACE BLOCKS

To facilitate development of software for MICRO computer on larger machines, a cross-assembler and a simulator written in FORTRAN-IV are available as a standard support software. A special version of simulator written in the assembly language of TDC-316, is also available.

The system features include a 78 basic instruction set with a variety of addressing modes, stack architecture, interrupt facility and DMA (Direct Memory Access) capability.

The bus signals and interface design rules are given in Appendix I.

3.2 PROGRAMMABLE PERIPHERAL INTERFACE (PPI)

The microcomputer communicates with the external world normally through the Teletype. However, to input the real-time variables (such as voltage and current in digital form) and to generate some control outputs (such as gain control) the user has to develop an 'interface' circuitry to meet his requirements. There are two types of Input/Output interfaces that can be used on an 8080 microprocessor-based computer. They are,

1. Memory Mapped I/O, and
2. Normal I/O.

The memory mapped I/O uses the memory read/write control signals and sits in the memory address space. In this, essentially, an I/O port is treated as a memory location, and hence all memory reference instructions can be used for I/O also.

However, the 8080 microprocessor also provides separate I/O controls and an 8-bit I/O address space. Thus the user can have 256 INPUT and 256 OUTPUT ports without reducing the memory space. Hence it was decided to make use of the I/O instructions and the I/O address space rather than a memory mapped I/O.

Figure 3.2 gives PPI card schematic diagram. The following design specifications are taken into account in designing the I/O interfaces :

1. It should be a general purpose card available to a variety of users.
2. It should provide flexibility for instrument modification/ expansion.

Hence the cards are made with the following capabilities :

1. They are relocatable anywhere in the I/O address space by means of manual switches.
2. Each PPI card provides three I/O ports to cater for sufficient I/O interfaces.
3. The mode of operation (INPUT or OUTPUT) of any particular port is decided by the user through software. For this

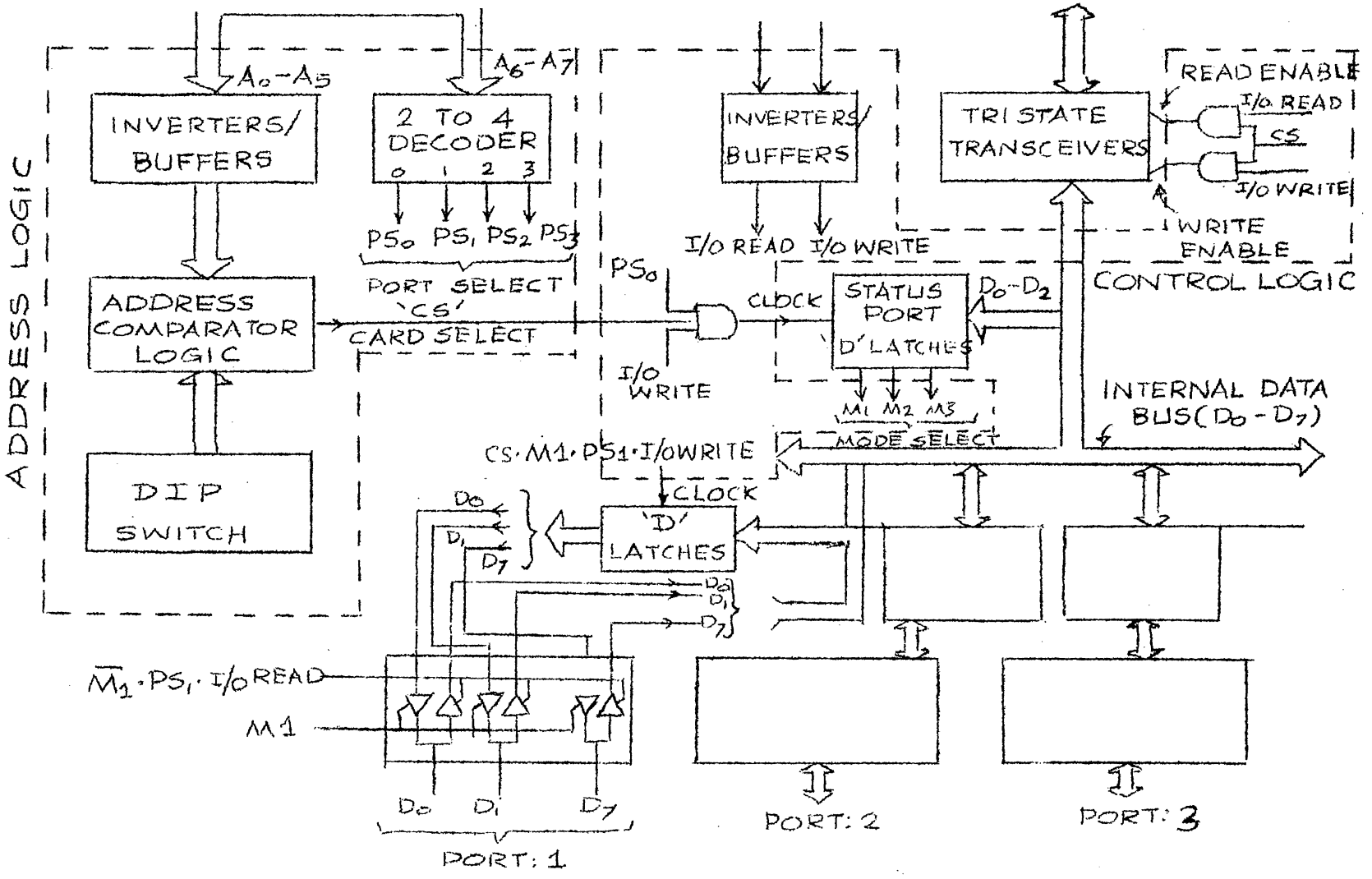


FIG 3·2: PROGRAMMABLE PERIPHERAL INTERFACE (PPI) CARD SCHEMATIC

purpose, a fourth port called 'STATUS PORT' is provided. The status port is the 'origin' (or displacement) of a particular PPI card in the I/O address space and the mode of operation of the next successive three ports are decided by what is written into the status port through software.

4. With 'power-on' and 'Master-clear' (from the microcomputer console) all the ports go into input mode so that accidental destruction due to two outputs clashing is avoided.

5. An interrupt line is also included to provide interrupt facility.

The data written on to a port remains valid till another data arrives at the same port. For this, latches are used in the output mode.

The address selection is made as follows :

The LSB 8-bits of the Address Bus are used by the computer for addressing in I/O instruction. In the PPI card of the 8-bits the LSB 6 bits are used for 'card select' and the remaining 2-bits are used for 'port-select'. By having a DIP switch an address comparison is made with the address on the address bus to give the 'card-select' signal. Now the remaining 2-bits will select a particular port (status port + 3 I/O ports) upon an I/O instruction. Thus the ports are relocatable anywhere in the I/O address space by altering the switch position on the DIP switch soldered on the interface card. These

interface cards directly go into the microcomputer bin. The INPUT/OUTPUT connections are through a 40 pin edge connector.

This type of design has proved very useful for a variety of users and also enhances the system flexibility.

Two such cards are made to interface DAC and ADC and to provide software gain control and start convert command. The allocation of different ports is shown in Table 3.1.

PORT No.	PROG. ADDRESS (Octal)	Bits Used	Bits Not Used	Mode	Purpose
1	371	0-7	None	Input	For LSB 8-bits of ADC
2	372	0-3	4-7	Input	For MSB 4-bits of ADC
3	373	0	1-7	Output	Start Convert
4	375	0-7	None	Output	For LSB 8-bits of DAC
5	376	0-3	4-7	Output	For MSB 4-bits of DAC
6	377	0-4	5-7	Output	For Gain Control

Table 3.1 Port Allocation

3.3 DIGITAL TO ANALOG CONVERTER (DAC) and DRIVER

As mentioned earlier, accuracy considerations demand a high resolution converter such as 10-bits or 12-bits. Availability of a 12-bit DAC was the deciding factor while choosing the DAC.

DA 1200 is a low cost, 12-bit digital-to-analog converter with a variety of input coding options. The input coding options include complementary binary and complementary BCD formats. In all instances, a logic 'low' ($\leq$ 0.8 V) turns a given bit ON, and a logic 'high' ($\geq$ 2.0 V) turns the bit OFF. Both current-and voltage-mode outputs are available with 1.5 μs and 2.5 μs settling time respectively. Output format may be programmed for bipolar ($\pm$ 10 V) or unipolar (0 to 10V) operations using internally supplied thin-film resistor pin strap options. The DAC is available in 24-pin Dual-in-Line Package (DIP).

For our application unipolar, voltage output mode (0-10 V) is chosen.

Since the DAC is a fast-settling one (2.5 μs), the associated Driver circuitry external to the chip is also made compatible.

The DAC and Driver circuitry along with gain control provisions are shown in Fig. 3.3.

The Driver circuit consists of a hybrid integrated circuit buffer having high input impedance, excellent slew rate and good current driving capability. This buffer (LH 0063,

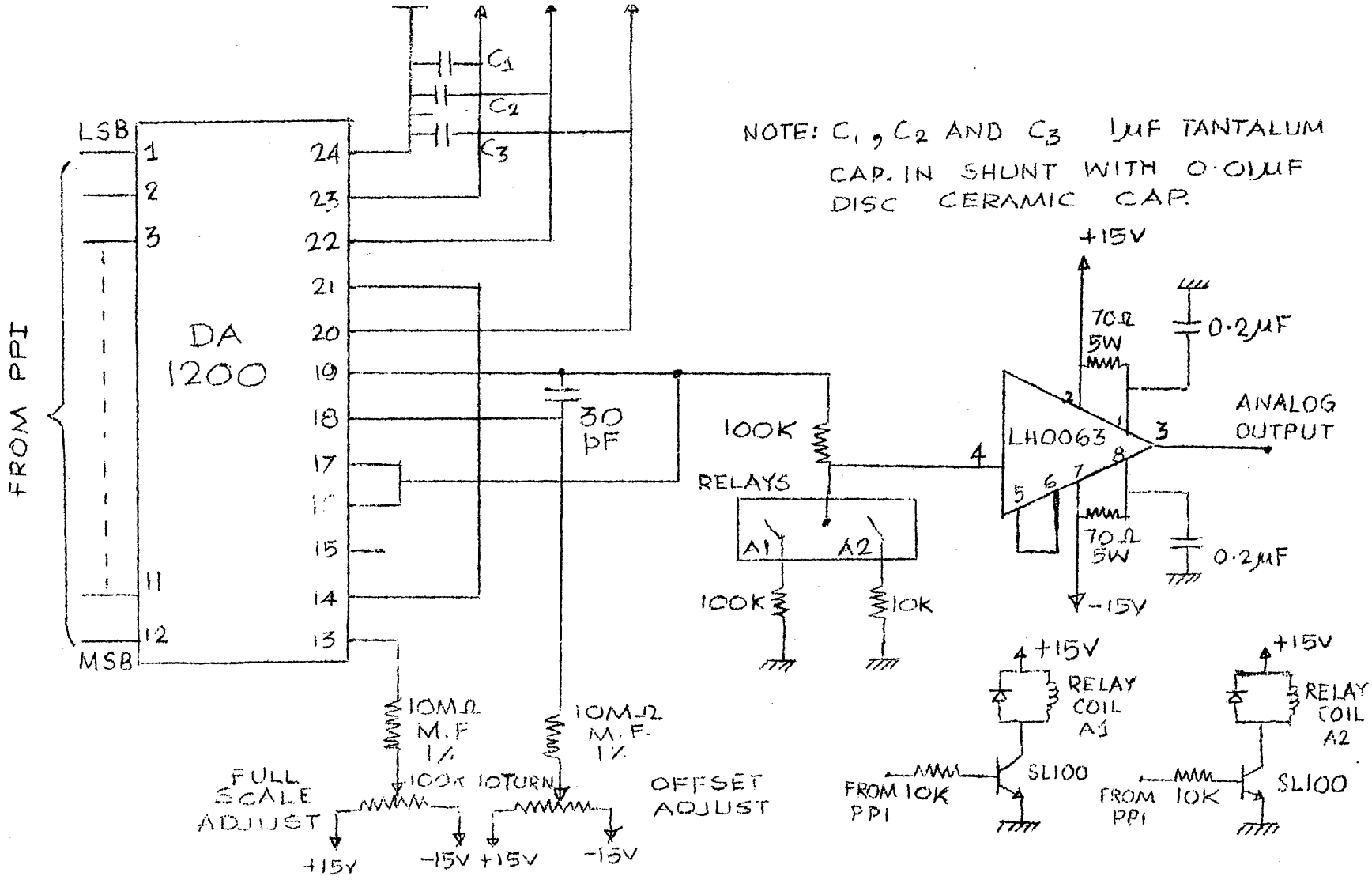


FIG 3.3: DIGITAL-TO-ANALOG CONVERTER AND DRIVER CIRCUIT

National Semiconductors) is a fast FET input buffer (unity gain) having current driving/sinking capability of 200 mA. The IC is laser trimmed for low off-set and has a slew-rate of 5000 Volts/μs. Short-circuit protection is provided by connecting external resistors in the output circuitry.

Gain control is achieved by relay switching of resistors at the output of DAC (or input of Driver). By generating appropriate commands (provided through software) user can select any of the following voltage ranges.

COMMAND	Voltage Range (Volts)
V = 1	0 - 10
V = 2	0 - 5
V = 3	0 - 1

In each of the ranges a maximum of 4096 steps can be given starting from 0 V to the maximum voltage. Hence, depending upon the sensitivity of the device under test, the user can select any desired range to get highly accurate I-V characteristics.

3.4 SENSOR CIRCUIT

The Sensor circuit is a current-to-voltage converter using op-amps. The choice of the op-amp is critical here from the input bias current point of view, as any bias current will result in error.

The Sensor circuit is shown in Fig. 3.4. It consists of a low cost, high accuracy, low input bias current (50 pA max.) FET input op-amp and gain control circuitry. The gain control circuitry consists of switchable precision metal film resistors, relays and relay drivers (open-collector TTL inverters).

Since the test device is connected between the output of the Driver and input of the Sensor op-amp (which is at virtual ground), the voltage output of the Driver essentially appears across the device. The device current flows thorugh the feed-back resistor in the Sensor circuit resulting in a voltage $V = IR$. This feed back resistor can be 'relay-switched' by software to give the desired gain. Two gain resistors (100 Ohms, 50 Ohms) are internally provided for the user. A third command open the feed-back path giving the user an option of plugging any resistor externally. Since the op-amp cannot supply the desired current (about 200 mA) external power transistors are provided for this purpose. The power transistors provided can give 3 amps (maximum).

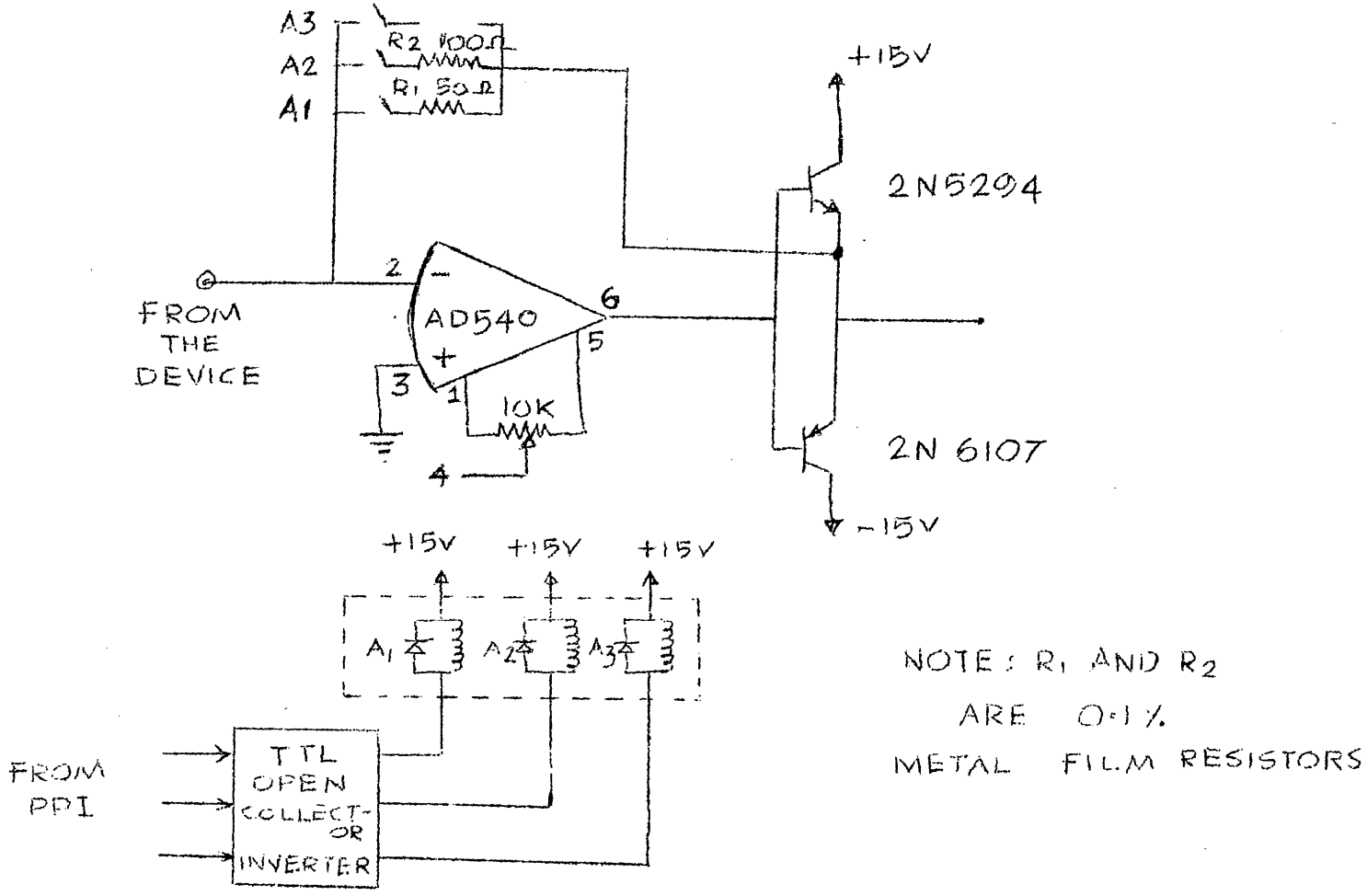


FIG 3·4: SENSOR CIRCUIT

3.5 SAMPLE-HOLD AND ANALOG-TO-DIGITAL CONVERTER CIRCUIT

The solar cell under illumination by a tungsten lamp has 50 Hz ripple in its output. Hence it is necessary to have a sample-hold circuit to hold the voltage during conversion time.

The sample-hold circuit along with the Analog-to-Digital converter and associated logic circuitry is shown in Fig. 3.5(a). Since high accuracy has to be retained throughout the system, high performance OP-AMPS are used.

The sample-hold circuit consists of a series switch element and a voltage translator to convert the TTL S/H commands from + 15 V to - 15 V for switching JFET. An output operational amplifier LM 308 buffers the sampled signal. When the logic input is '1' the control voltage switches to - 15 V and the FET is OFF and the storage capacitor C1 holds the signal voltage. The sampling element is a JFET 2N 4393. It features a low I_{DSS} (5 nA) and in the hold mode has a low drift rate of 3 μV/sec when a 0·1 μF hold capacitor is used. An isolation resistor R1 included between the capacitor C1 and the input of LM 308 insures that the op-amp will not be damaged by shorting at the output or abruptly shutting down the power supplies when the capacitor is charged.

The ADC is a 12 bit monolithic CMOS converter working on charge balance principle. The converter, ADC-EK 12 B, is a low

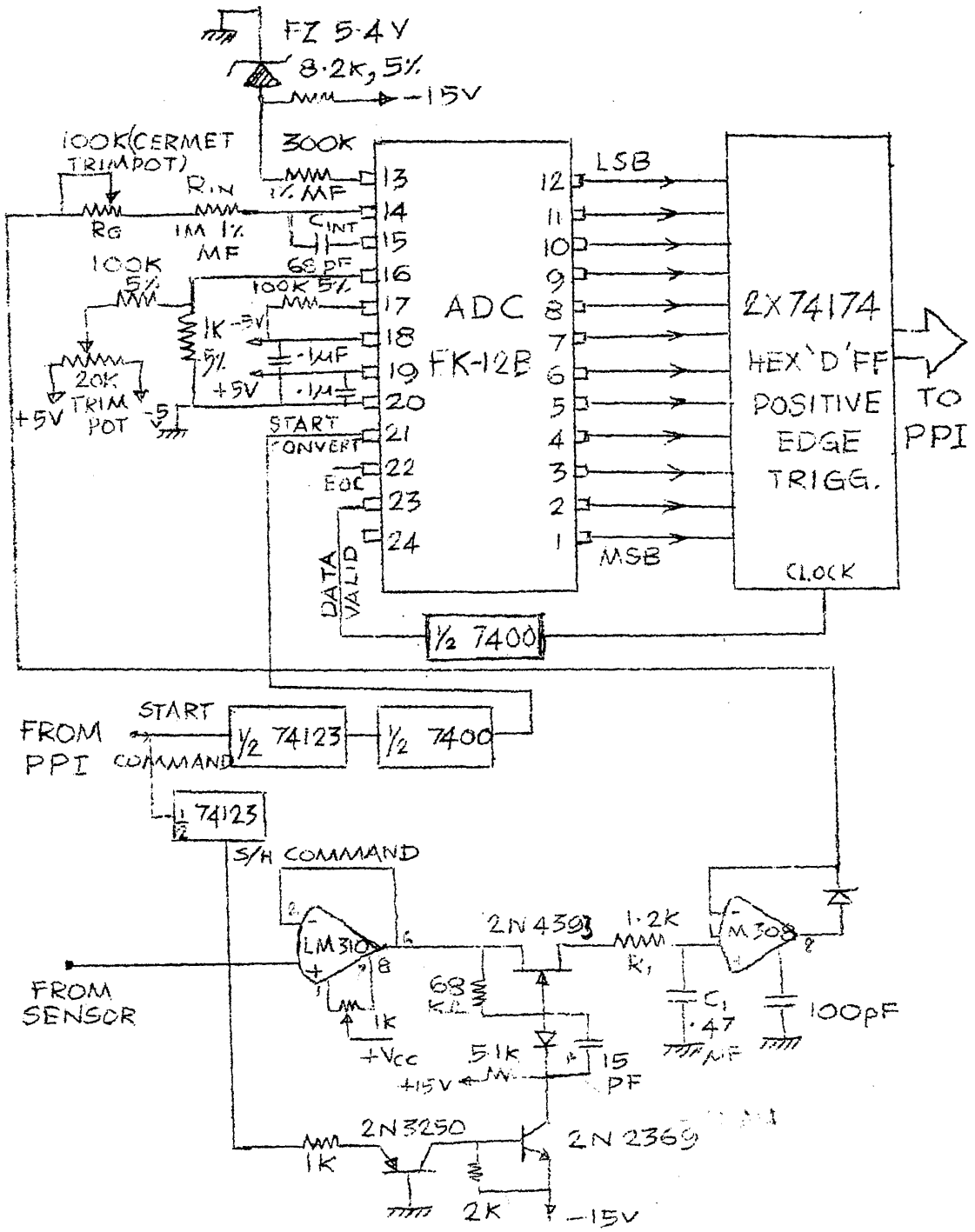
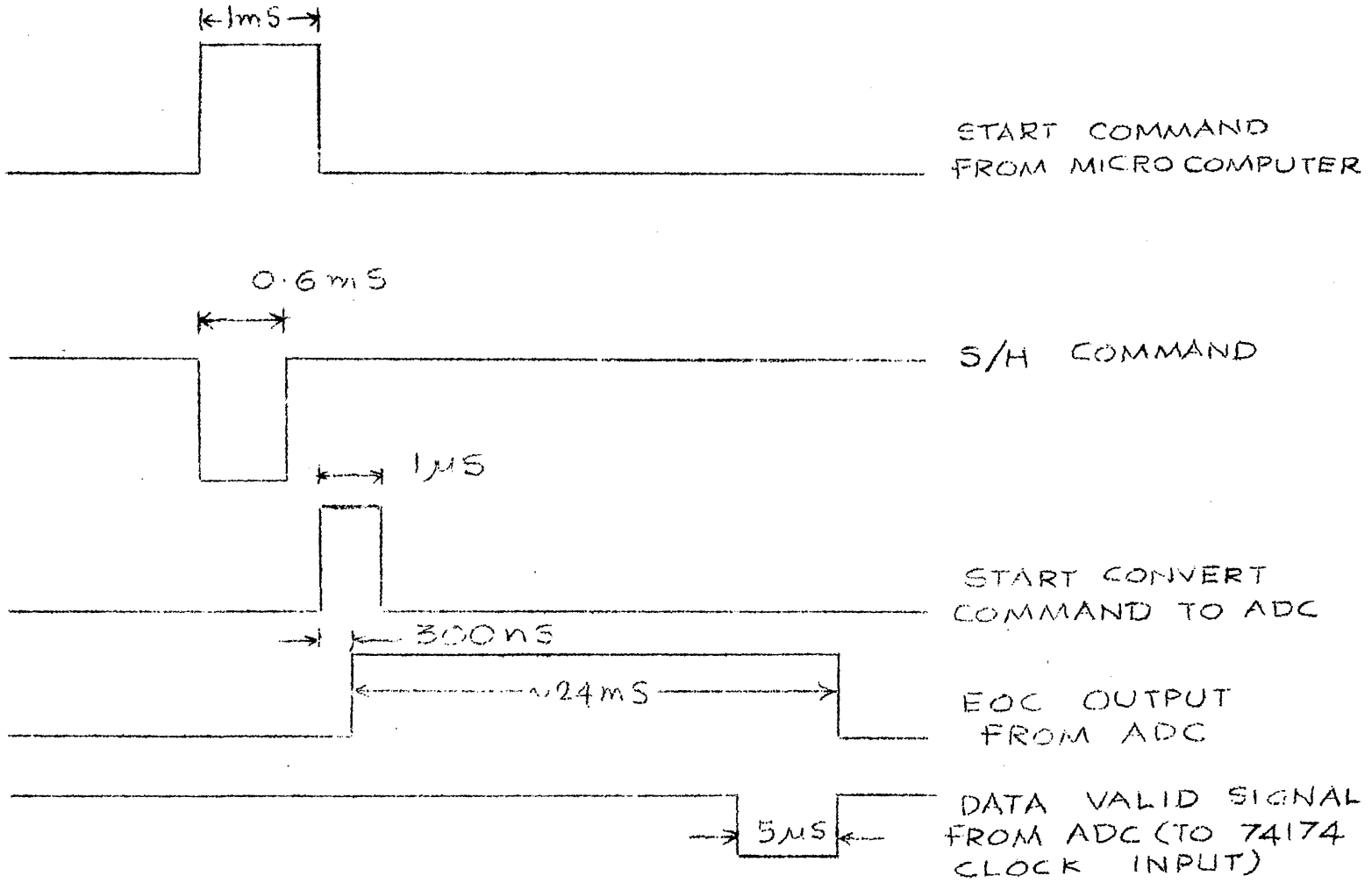


FIG 3.5 a: SAMPLE-HOLD AND ANALOG-TO-DIGITAL CONVERTER CIRCUIT

FIG 3-5 b: SAMPLE-HOLD AND ADC TIMING LOGIC



power, integrating type CMOS monolithic chip with 12-bit accuracy. It features 20 milliwatt power consumption with no missing codes and low cost. The charge balancing integration technique gives high linearity along with inherent monotonicity resulting in no missing codes. The output data appears in parallel form (TTL compatible). The conversion time is 24 msec (max.) and analog input voltage range is programmable by means of an external resistor. Standard operating mode is unipolar but bipolar operation can be realized using an external op-amp[6].

The conversion logic signal generation is as follows :

1. The microcomputer generates a 1 msec pulse through its output port.
2. The leading edge of the pulse is used for sampling the analog voltage. The sample time is 0.6 msec.
3. The falling edge is used to give a 'start convert' command for the ADC. This is generated by a monostable giving 'start convert' pulse of 1 μs.

The logic is illustrated in Fig. 3.5(b).

The conversion time is about 24 msec and at the end of it, , the ADC acknowledges with a low-to-high transition 'DATA VALID' signal. This signal latches the data into dual hex latches and is taken in by the microcomputer before giving the next 'start convert' command.

3.6 SOFTWARE ORGANIZATION

As noted earlier, the software has to

1. provide data averaging,
2. be capable of detecting sensitive regions in the I-V characteristics,
3. accept gain control commands and set gains accordingly,
4. give the data in a user readable, easy-to-follow tabular format,
5. provide modularity and facilitate future modifications.

The software, written in the assembly language of MICRO-78 has twenty subroutines and one main routine (which links all the subroutines). The total program area is about 2K which can be stored in ROM in case of a dedicated system, and a data area, the size of which will depend on the device under test. Maximum data area is about 1.5 K which is semiconductor RAM. The program uses Stack Area for temporary storage and subroutine call and return.

Fig. 3.6 illustrates the flow chart of the program. Note that the voltage and the corresponding current values are stored in the memory to facilitate any further processing of the data. For every voltage setting a pair of current readings are taken, averaged and printed. Four such pairs are taken and the average of all the averaged pairs is also printed. Two successive current values are compared while deciding the

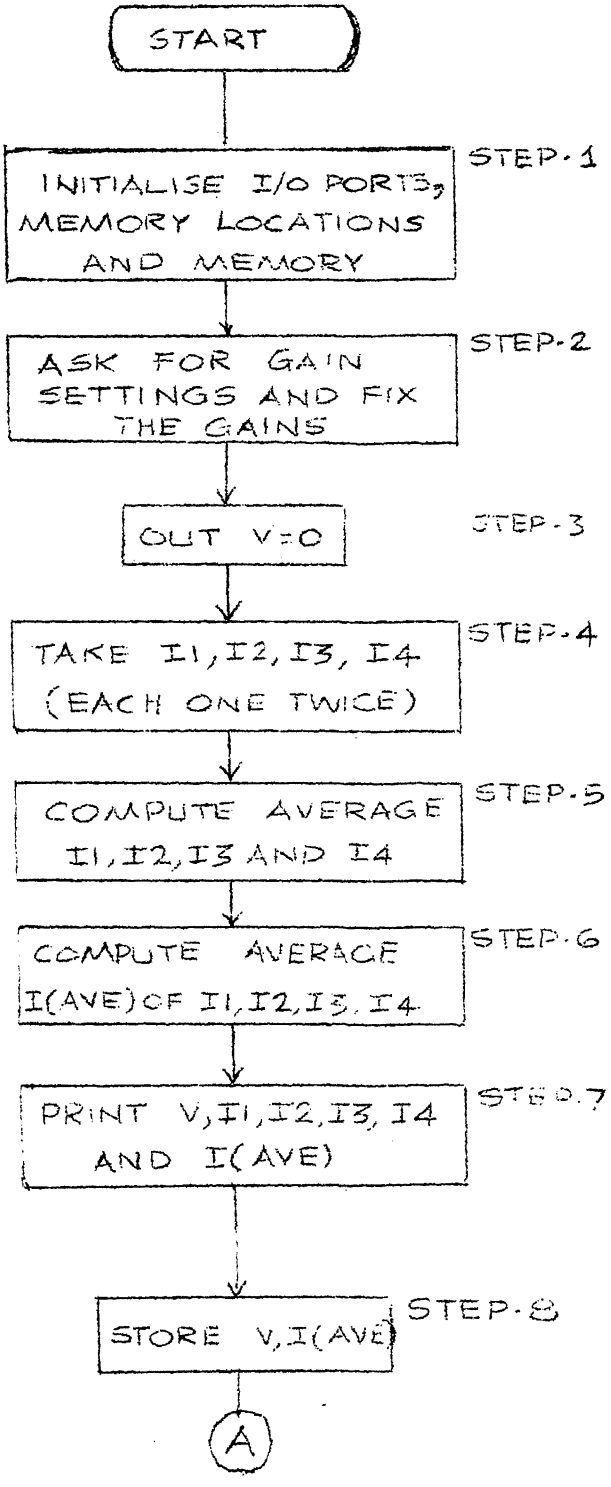


FIG 3·6: FLOW CHART OF THE PROGRAM

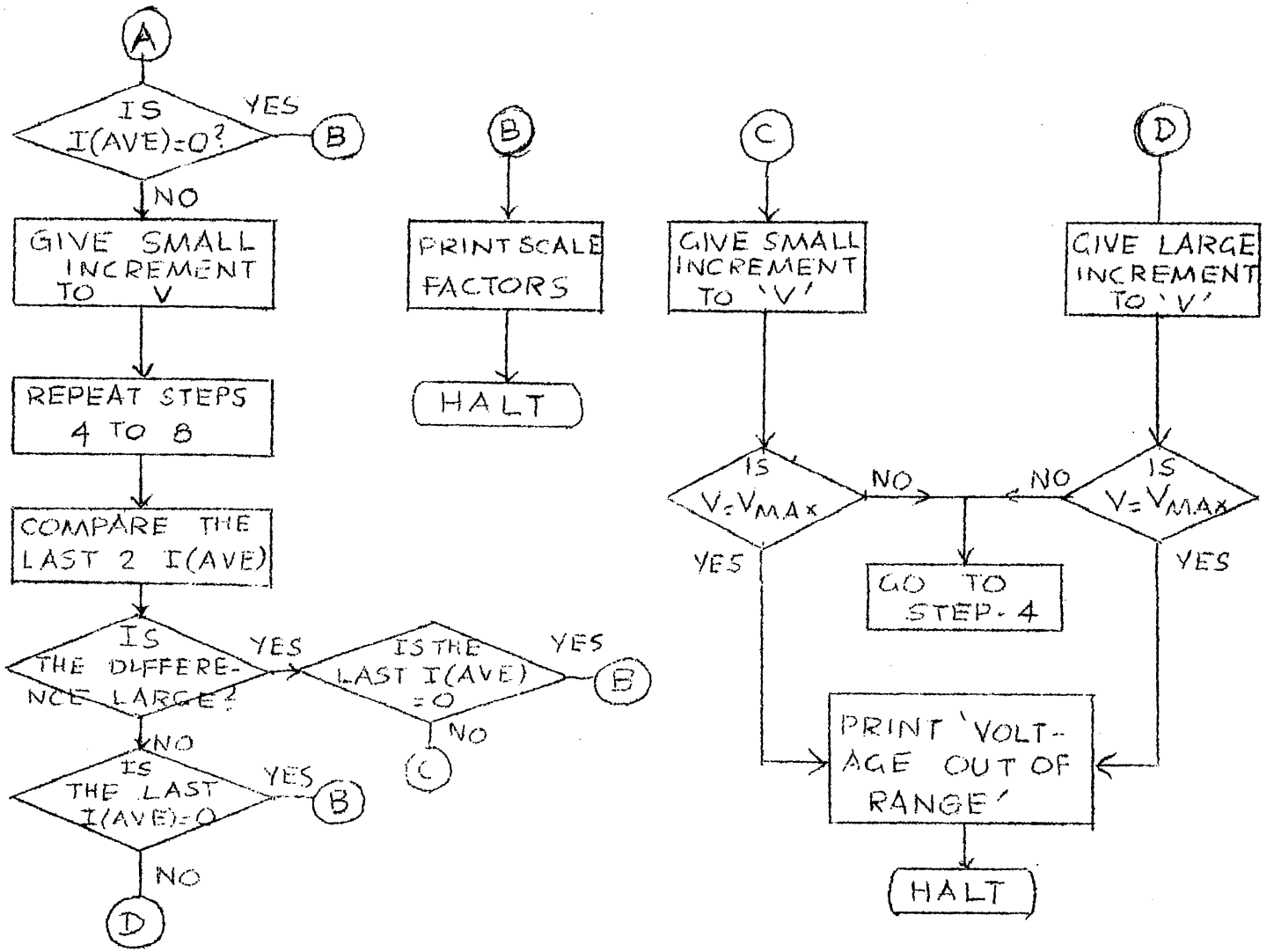


FIG 3·6: FLOW CHART OF THE PROGRAM

next voltage setting. A large difference will result in a smaller voltage increment for the next step and small difference in two successive readings will result in a larger voltage increment. The amount of difference in current readings and the voltage increments to be applied are user selectable in software.

Thus the software routine can cater for I-V measurement of any two-terminal device. However, since the ADC cannot sense negative voltages (negative voltage will result if the device under test is not a generator, as the current direction will be now opposite) an inverter is provided in the hardware to meet the need. Now, the output of the Sensor has to go through the inverter to the ADC for measurement.

The I-V data accessed for a solar cell are given in the next chapter. The readings include conditions of different illuminations and in dark; I-V data accessed for an ordinary diode are also presented.

A complete listing of the software is given in Appendix II.

CHAPTER 4

RESULTS AND DISCUSSION

With the instrument fully operational, I-V characteristics of a solar cell (illuminated and dark) and an ordinary diode (forward bias) were taken, Sample readings are given in Tables 4.1 to 4.5.

The solar cell I-V curves under two different illumination levels are plotted and an approximate calculation of series resistance is carried out as shown in the graph (Fig. 4.1)[7]. The method adopted is as follows :

Considering the effect of series resistance alone, the I-V relationship of a solar cell at light intensity L_1 is,

$$I_1 = I_o \left[e^{\frac{q}{AkT}(V_1 - I_1 R_s)} - 1 \right] - I_{L_1} \qquad (4.1)$$

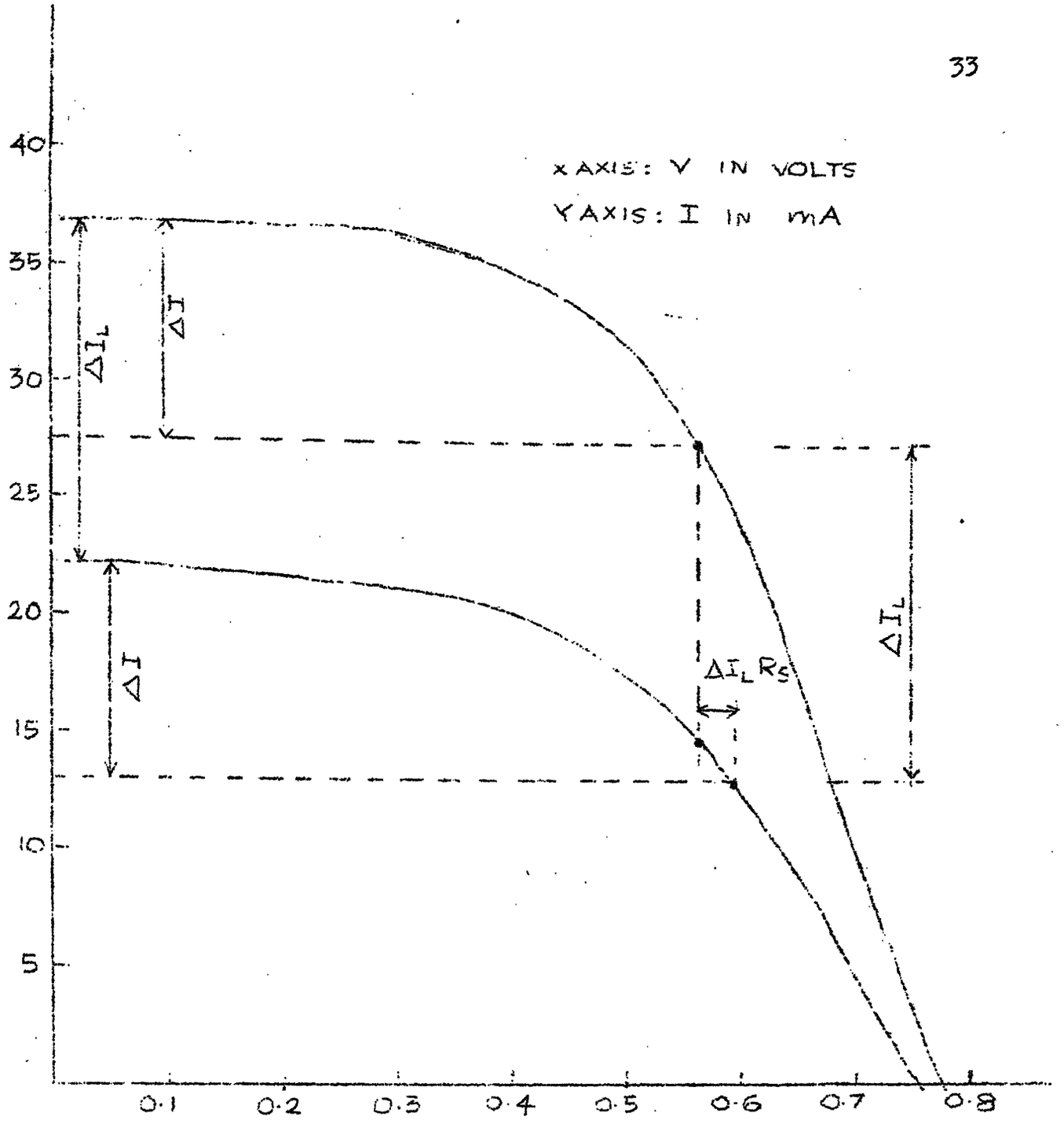
at light intensity L_2,

$$I_2 = I_o \left[e^{\frac{q}{AkT}(V_2 - I_2 R_s)} - 1 \right] - I_{L_2} \qquad (4.2)$$

when parameters have the usual notations.

Since I_L is a constant current source proportional to the light intensity, I_{L_2} can be expressed as,

$$I_{L_2} = I_{L_1} + \Delta I_L \qquad (4.3)$$



SOLAR CELL I-V UNDER TWO DIFFERENT ILLUMINATION AND APPROXIMATE SERIES RESISTANCE CALCULATION

Fig. 4.1

Since the voltage is an independent variable, if we choose

$$V_1 - I_1 R_s = V_2 - I_2 R_s \qquad (4.4)$$

eqn. (4.1) minus (4.2) gives,

$$I_1 - I_2 = \Delta I_L \qquad (4.5)$$

Equation (4.5) in (4.4) gives,

$$V_1 - V_2 = \Delta I_L R_s \qquad (4.6)$$

where V_1 and V_2 are the terminal voltages.

Using this, R_s can be found out graphically as illustrated. For the I-V characteristics drawn, R_s = 2.0 Ohms.

As such a better way of finding out the series resistance and other parameters of the solar cell or any other device will be through curve fitting programs on a larger computer. Since the main aim of the project was to construct an I-V data acquisition system, this work was not carried out. However the linearity and the correctness of the instrument were verified using direct calibration procedures.

Since the instrument treats the device as a 'black-box' I-V characteristics of any type of solar cell (p-n junction, hetero-junction, amorphous or MOS types) or any other two terminal device can be carried out without any problem. It is to be noted that for other devices, (say p-n junction diode or

schottky-barrier diode or solar cell in dark) the inverter should be also included in the signal path from sensor to ADC input; in software the required modification is to load γ'NOP' (No operation) code (000) into locations 206, 207, 210, 231, 232 and 233 (octal addresses).

From the I-V data one can realize that close-spaced points are taken in pairs in the sensitive regions. In the not so sensitive regions instead of close-spaced pairs of data, larger voltage steps are given. The software can be modified to take more number of data in the sensitive regions rather than close-spaced points in pairs (with larger displacement between two such pairs. By pairs we mean two successive I (average) readings): this could be achieved by a dynamic computation of step size and back-tracking capability. This modification is however not implemented on the present set-up.

V=1,I=3 TABLE 4.1 SOLAR CELL I-V

V	I1	I2	I3	I4	I(AVE)
0000	3680	3715	3685	3671	3687
0002	3719	3685	3667	3673	3685
0021	3721	3656	3648	3692	3678
0041	3662	3699	3712	3704	3695
0060	3676	3715	3699	3665	3687
0080	3712	3680	3658	3653	3676
0099	3706	3673	3662	3682	3680
0119	3660	3667	3699	3719	3685
0138	3653	3701	3690	3699	3685
0158	3678	3704	3692	3667	3685
0177	3687	3690	3667	3651	3673
0197	3687	3682	3667	3641	3667
0216	3682	3687	3665	3653	3671
0236	3671	3697	3687	3646	3676
0255	3667	3697	3676	3658	3673
0275	3651	3673	3653	3621	3648
0294	3651	3646	3628	3598	3628
0314	3637	3617	3595	3593	3609
0333	3637	3584	3568	3587	3593
0353	3609	3554	3556	3578	3573
0372	3554	3526	3548	3593	3554
0392	3524	3520	3545	3550	3534
0411	3463	3490	3504	3500	3487
0431	3422	3463	3458	3433	3444
0450	3412	3387	3366	3355	3380
0470	3334	3272	3290	3309	3300
0473	3302	3275	3309	3327	3302
0492	3197	3249	3258	3233	3233
0512	3132	3136	3109	3085	3113
0514	3134	3090	3079	3094	3099
0533	2989	2953	2968	2992	2975
0535	2934	2959	2989	2989	2968
0555	2799	2840	2836	2817	2821
0557	2823	2797	2762	2775	2789
0576	2633	2592	2611	2628	2617
0579	2574	2599	2613	2624	2602
0599	2384	2412	2412	2396	2401
0601	2367	2371	2348	2334	2354
0620	2159	2118	2114	2135	2130
0625	2125	2096	2111	2133	2116
0644	1842	1884	1896	1889	1877
0646	1817	1851	1844	1826	1835
0666	1573	1569	1544	1534	1553
0669	1532	1505	1493	1493	1505
0688	1243	1210	1204	1212	1217
0690	1199	1165	1173	1180	1178
0710	0894	0880	0898	0907	0894
0712	0859	0861	0873	0880	0868
0731	0570	0579	0585	0596	0581
0733	0581	0548	0557	0555	0548
0753	0250	0273	0278	0269	0267
0756	0214	0241	0243	0228	0230
0775	0021	0028	0024	0019	0021
0777	0011	0014	0014	0011	0011
0797	0000	0000	0000	0000	0000

MULTIPLICATION FACTORS:
FOR V=1 USE [1.0E-03] V-IN VOLTS
FOR I=3 USE [1/R(1.0E-03)] R=100 OHMS I-IN AMPS.

V	I1	I2	I3	I4	I(AVE)
0000	2174	2213	2196	2187	2192
0002	2203	2189	2174	2176	2183
0021	2192	2176	2192	2196	2189
0041	2164	2189	2194	2189	2183
0060	2192	2187	2162	2155	2172
0080	2194	2153	2159	2174	2169
0099	2155	2164	2192	2183	2172
0119	2183	2172	2155	2159	2167
0138	2159	2167	2187	2181	2172
0158	2174	2169	2148	2150	2159
0177	2150	2144	2169	2181	2159
0197	2150	2176	2159	2137	2155
0216	2164	2137	2139	2159	2150
0236	2128	2164	2164	2144	2150
0255	2155	2139	2123	2125	2135
0275	2116	2116	2130	2144	2125
0294	2109	2135	2135	2123	2125
0314	2123	2114	2094	2094	2105
0333	2096	2079	2094	2111	2094
0353	2059	2096	2091	2064	2077
0372	2084	2047	2045	2055	2057
0392	2018	2038	2052	2042	2038
0411	2003	2025	1999	1997	2006
0431	1983	1955	1955	1967	1964
0450	1910	1925	1942	1938	1928
0470	1877	1886	1877	1861	1875
0489	1831	1807	1810	1826	1817
0509	1714	1762	1759	1746	1744
0528	1684	1664	1649	1656	1661
0531	1661	1640	1659	1673	1656
0551	1549	1578	1578	1562	1567
0553	1573	1549	1544	1562	1556
0572	1439	1466	1464	1452	1454
0574	1456	1439	1430	1439	1439
0594	1308	1335	1342	1328	1328
0596	1324	1305	1294	1305	1305
0615	1165	1187	1199	1185	1182
0618	1180	1156	1146	1160	1160
0639	1009	1024	1034	1034	1024
0641	1009	1004	0985	0990	0997
0660	0841	0836	0848	0859	0846
0664	0814	0831	0820	0807	0816
0683	0660	0641	0646	0664	0651
0685	0615	0639	0639	0630	0630
0705	0459	0440	0436	0440	0443
0708	0423	0414	0436	0438	0425
0727	0241	0255	0248	0241	0245
0729	0243	0221	0225	0236	0230
0749	0053	0060	0065	0063	0060
0751	0046	0048	0044	0046	0046
0770	0000	0000	0000	0000	0000

MULTIPLICATION FACTORS:
FOR V=1 USE [1.0E-03] V-IN VOLTS
FOR I=3 USE [1/R(1.0E-03)] R=100 OHMS I-IN AMPS.

V=1,I=3 TABLE 4.3 SOLAR CELL I-V

V	I1	I2	I3	I4	I(AVE)
[illegible]	[illegible]	0604	0601	0599	0601
[illegible]	1.601	0601	0599	0594	0599
0081	0604	0596	0594	0594	0596
[illegible]	0601	0594	0592	0594	0594
[illegible]	0599	0592	0590	0596	0592
[illegible]	0596	0592	0593	0587	0596
0099	0596	0594	0596	0596	0592
0119	0594	0596	0592	0590	0592
0138	0592	0594	0592	0587	0591
0158	0594	0587	0585	0587	0587
0177	0596	0581	0585	0590	0585
0197	0581	0581	0585	0587	0581
0216	0576	0581	0585	0587	0581
0236	0572	0581	0579	0576	0576
0255	0572	0576	0574	0570	0572
0275	0572	0572	0567	0565	0567
0294	0565	0565	0560	0557	0560
0314	0557	0557	0555	0553	0555
0333	0551	0551	0548	0542	0548
0353	0542	0542	0537	0535	0537
0372	0531	0531	0526	0523	0526
0392	0518	0514	0509	0509	0512
0411	0503	0496	0494	0492	0496
0431	0482	0477	0473	0475	0475
0450	0457	0443	0450	0450	0450
[illegible]	0431	0423	0429	0431	0429
0470	0397	0397	0399	0414	0399
0509	0358	0360	0362	0365	0360
0528	0319	0321	0326	0328	0320
0548	0275	0275	0275	0273	0275
0567	0225	0221	0223	0225	0223
0587	0172	0165	0167	0167	0167
0606	0113	0104	0102	0104	0104
0627	0046	0039	0039	0035	0039
0646	0002	0000	0000	0000	0000

MULTIPLICATION FACTORS:
FOR V=1 USE [1.0E-03]
FOR V=2 USE [5.5E-03] V-IN VOLTS
FOR V=3 USE [1.0E-04]
FOR I'S USE [1/R(1.0E-03] I-IN AMPS.
WHERE R IS IN OHM(100)

V=1,I=3 TABLE 4.4 SOLAR CELL I-V(DARK)

V	I1	I2	I3	I4	I(AVE)
0008	0001	0000	0000	0000	0000
0021	0001	0000	0000	0000	0000
0041	0001	0000	0000	0000	0000
0061	0001	0000	0000	0000	0000
0080	0001	0000	0000	0000	0000
0099	0001	0000	0000	0000	0000
0119	0001	0000	0000	0000	0000
0138	0001	0000	0000	0000	0000
0158	0001	0000	0000	0000	0000
0177	0001	0000	0000	0000	0000
0197	0001	0000	0000	0000	0000
0216	0002	0002	0002	0002	0002
0236	0005	0005	0005	0005	0005
0255	0009	0009	0009	0009	0009
0275	0014	0014	0014	0014	0014
0294	0019	0019	0019	0019	0019
0314	0026	0026	0026	0026	0026
0333	0033	0033	0033	0033	0033
0353	0041	0041	0041	0041	0041
0372	0050	0050	0050	0050	0050
0392	0063	0063	0063	0063	0063
0411	0072	0072	0072	0072	0072
0431	0087	0087	0087	0087	0087
0450	0102	0102	0102	0102	0102
0470	0119	0119	0119	0119	0119
0489	0138	0138	0138	0138	0138
0509	0161	0161	0161	0161	0161
0528	0184	0184	0184	0184	0184
0548	0214	0214	0214	0214	0214
0567	0245	0245	0245	0245	0245
0587	0280	0280	0280	0280	0280
0606	0321	0321	0321	0321	0321
0627	0362	0365	0365	0365	0362
0646	0414	0414	0414	0414	0414
0666	0470	0470	0470	0470	0470
0685	0533	0533	0533	0533	0533
0705	0604	0604	0604	0604	0604
0724	0683	0683	0683	0683	0683
0744	0770	0772	0772	0772	0770
0747	0783	0783	0783	0783	0783

MULTIPLICATION FACTORS:
FOR V=1 USE [1.0E-03] V-IN VOLTS
FOR I=3 USE [1/F(1.0E-03)] R=1000 OHMS I-IN AMPS.

V=1,I=0 TABLE 4.5 I-V OF A POWER DIODE(70 MIL 100A)

V	I1	I2	I3	I4	I(AVE)
0002	0000	0000	0000	0000	0000
0042	0000	0000	0000	0000	0000
0081	0000	0000	0000	0000	0000
0121	0000	0000	0000	0000	0000
0160	0000	0000	0000	0000	0000
0200	0000	0000	0000	0000	0000
0239	0000	0000	0000	0000	0000
0279	0000	0000	0000	0000	0000
0319	0000	0000	0000	0000	0000
0358	0000	0000	0000	0000	0000
0398	0000	0000	0000	0000	0000
0437	0000	0000	0000	0000	0000
0477	0000	0000	0000	0000	0000
0517	0000	0000	0000	0000	0000
0556	0000	0000	0000	0000	0000
0596	0000	0000	0000	0000	0000
0635	0000	0000	0000	0000	0000
0675	0000	0000	0000	0000	0000
0715	0000	0000	0000	0000	0000
0754	0000	0000	0000	0000	0000
0794	0000	0000	0000	0000	0000
0834	0000	0000	0000	0000	0000
0873	0000	0000	0000	0000	0000
0913	0000	0000	0000	0000	0000
0952	0000	0000	0000	0000	0000
0992	0000	0000	0000	0000	0000
1032	0000	0000	0000	0000	0000
1071	0000	0000	0000	0000	0000
1111	0000	0000	0000	0000	0000
1150	0000	0000	0000	0000	0000
1190	0000	0000	0000	0000	0000
1230	0000	0000	0000	0000	0000
1269	0000	0000	0000	0000	0000
1309	0000	0000	0000	0000	0000
1348	0000	0000	0000	0000	0000
1388	0000	0000	0000	0000	0000
1428	0000	0000	0000	0000	0000
1467	0000	0000	0000	0000	0000
1507	0000	0000	0000	0000	0000
1547	0000	0000	0000	0000	0000
1586	0000	0000	0000	0000	0000
1626	0000	0000	0000	0000	0000
1665	0000	0000	0000	0000	0000
1705	0000	0000	0000	0000	0000
1745	0000	0000	0000	0000	0000
1784	0000	0000	0000	0000	0000
1824	0000	0000	0000	0000	0000
1864	0000	0000	0000	0000	0000
1903	0000	0000	0000	0000	0000
1943	0000	0000	0000	0000	0000
1983	0000	0000	0000	0000	0000
2022	0000	0000	0000	0000	0000
2062	0000	0000	0000	0000	0000
2101	0000	0000	0000	0000	0000
2141	0000	0000	0000	0000	0000
2181	0000	0000	0000	0000	0000
2220	0000	0000	0000	0000	0000
2260	0000	0000	0000	0000	0000
2299	0000	0000	0000	0000	0000
2339	0000	0000	0000	0000	0000
2379	0000	0000	0000	0000	0000
2418	0000	0000	0000	0000	0000
2458	0000	0000	0000	0000	0000
2498	0000	0000	0000	0000	0000
2537	0000	0000	0000	0000	0000
2577	0000	0000	0000	0000	0000
2617	0000	0000	0000	0000	0000
2656	0000	0000	0000	0000	0000
2696	0000	0000	0000	0000	0000
2735	0000	0000	0000	0000	0000
2775	0000	0000	0000	0000	0000
2815	0000	0000	0000	0000	0000
2854	0000	0000	0000	0000	0000
2894	0000	0000	0000	0000	0000
2934	0000	0000	0000	0000	0000
2973	0000	0000	0000	0000	0000
3013	0000	0000	0000	0000	0000
3052	0000	0000	0000	0000	0000
3092	0000	0000	0000	0000	0000
3132	0000	0000	0000	0000	0000
3171	0000	0000	0000	0000	0000
3211	0000	0000	0000	0000	0000
3251	0000	0000	0000	0000	0000
3290	0000	0000	0000	0000	0000
3330	0000	0000	0000	0000	0000
3369	0000	0000	0000	0000	0000
3409	0000	0000	0000	0000	0000
3449	0000	0000	0000	0000	0000
3488	0000	0000	0000	0000	0000
3528	0000	0000	0000	0000	0000
3568	0000	0000	0000	0000	0000
3607	0000	0000	0000	0000	0000
3647	0000	0000	0000	0000	0000
3687	0000	0000	0000	0000	0000
3726	0000	0000	0000	0000	0000
3766	0000	0000	0000	0000	0000
3805	0000	0000	0000	0000	0000
3845	0000	0000	0000	0000	0000
3885	0000	0000	0000	0000	0000
3924	0000	0000	0000	0000	0000
3964	0000	0000	0000	0000	0000
4004	0000	0000	0000	0000	0000

SCALE FACTORS:
FOR V=1 USE [1.0E-03] V-IN VOLTS
FOR I=0 USE [1/R(1.0E-03)] I=100 OHMS I-IN AMPS.

CHAPTER 5

CONCLUSION

A basic microprocessor-based solar cell data acquisition system has been built and tested. The present set-up is capable of taking the I-V data of solar cells under illumination and in dark. It can acquire I-V data of diodes also. It is possible to get the spectral response of the solar cells if monochromatic light sources are made available. More sophisticated hardware and software build-up over the existing one can make the instrument general-purpose and more powerful.

Software modifications require a knowledge of assembly language programming which is a constraint of the microcomputer-based instrument. It is expected that in future higher level languages will be operational with the microcomputer.

The modularity of the instrument set-up will facilitate future modifications and extensions. A user manual is being prepared for this purpose. Suggested enhancement of the facilities are : 1) incorporation of another DAC to take the I-V of three terminal devices and a C-V measurement unit along with necessary software 2) computation of the device parameters through software implementation in the microcomputer.

REFERENCES

1. Patrick H. Garrett, Analog Systems for Microprocessors and Minicomputers, Reston Publishing Co., Virginia, 1978.
2. R. Schultz, et. al., 'A Microprocessor-based Solar Cell Test System', IEEE Trans. on Instrumentation and Measurement, Vol. IM-26, No.4, Dec. 1977.
3. Luis Castaner et. al., 'Microprocessor-based Solar Cell Measurement System', IEEE Trans. on Instrumentation and Measurement, Vol. IM-27, No.2, June, 1978, pp. 152-156.
4. Amphenol, Product Catalog, Amphenol Sales Division, Columbus, 12020, USA, 1976.
5. DATEL, ADC-EK Series Manual.
6. Charles E. Backus, 'Solar Cells', IEEE Press, 1976, pp. 146-168.
7. MICRO-78 User's Manual.

APPENDIX - I

MICRO-78 BUS SIGNALS AND INTERFACE DESIGN RULES

The microcomputer I/O bus consists of 33 signals. The basic mechanical frame has 11 slots for standard 3 Ht. cards. The CPU module occupies one position and the remaining 10 positions can be used for Memory and I/O controller modules. The I/O signals run like a bus on back panel mother-board. Each of the 33 signals is allotted a particular pin in all the 11 positions. Hence the required signal for a particular pin can be tapped from the corresponding pin in that slot. In all, each slot has 120 pins. The total number of free pins available in each slot is 75. These pins can be used for inter-module wiring for those controllers which require more than one card. The device cables can be connected to a connecter mounted on the main frame through an adapter from the free edge of the card. All signals should be driven by open collectors or tristate buffers on the bus.

INPUT/OUTPUT INTERFACE SIGNALS

The following are the 33 I/O signals

S.No.	Name	Description	Logic	No. of lines
1	Add_0 to Add_{15}	Address Lines	-ve	16
2	D_0-D_7	Data lines	-ve	8
3	WXM	Write pulse for memory	-ve	1
4	WXO	Write pulse for I/O (0.48 to 2 μs)	-ve	1
5	TSRM	Read pulse for memory	-ve	1
6	TSRI	Read pulse for I/O	-ve	1
7	SSYN	Synchronizing signal from memory, indicating that a memory read/write is completed	-ve	1
8	IR	Interrupt request	-ve	1
9	DMAR	DMA request	-ve	1
10	DMAA	Acknowledge for DMAR	-ve	1
11	MC	Master clear signal issued by CPU to initiate some flags and registers in the device controllers	-ve	1

For more details user has to refer to the MICRO-78 system reference manual.

APPENDIX - II

SOURCE PROGRAM LISTING

```
COMND   SET     1117B
        ORG     100B
        LXI     SP, 5500B
        LXI     H, 3000B
        SHLD    AN
        LXI     H,3500B
        SHLD    ARAM
        LXI     H,4000B
        SHLD    TV
        MVI     A,0
        LXI     H,LF
        MOV     M,A
        XRA     A
        OUT     374B
        MVI     A,3
        OUT     370B
        CALL    COMND   : USER COMMAND FOR GAIN SETTING
        CALL    GAINS
        CALL    PRIN1
        LXI     H,5200B
        LXI     B,7777B
        CALL    DACO    : DAC OUTPUT ROUTINE
        CALL    DACS    : DAC SAVE ROUTINE
        CALL    ADCAV   : ADC AVERAGE ROUTINE
        CALL    ACHEK   : ADC CHECK ROUTINE
        JZ      LINE
AG:     DCX     B
        CALL    DACC    : DAC CHECK ROUTINE
        JZ      OFLOW
```

```
        CALL    CACO
        CALL    ADCAV
        CALL    ACHEK
        JZ      LINE
        CALL    PAT
        JNC     AG
        MVI     D, 7B
OG  :   DCX     B
        CALL    DACC
        JZ      OFLOW
        DCR     D
        JNZ     OG
        JMP     AG
OFLOW:  MVI     B,30
FL1 :   CALL    LFCR
        LXI     H, INFOM
        MOV     A,M
        CALL    OUTP
        DCR     B
        INX     H
        JNZ     FL1
LINE:   CALL    LFCR
        MV1     B,57B
        MVI     A,55B
LINE1 : CALL    OUTP
        DCR     B
        JNZ     LINE1
        CALL    LFCR
        MVI     C,6
        MVI     B,25
LINE2 : LXI     H,MULF
HERE :  MOV     A,M
        CALL    OUTP
```

```
        INX     H
        DCR     B
        JNZ     HERE
        CALL    LFCR
        DCR     C
        MVI     B,25
        JNZ     HERE
INFOM:  DA      OUT OF RANGE.CHANGE VOLTAGE GAIN
MULF:   DA      MULTIPLICATION FACTORS :
GULT:   FOR V=1 USE [1.0E-03]
        FOR V=2 USE [0.5 E-03]
        FOR V=3 USE [1.0 E-04]
        FOR I'S USE [1/R (1.0E - 03)]
        WHERE R IS IN OHMS
LFCR    MVI     A,15B
        CALL    OUTP
        MVI     A,12B
        CALL    OUTF
        RET
        ORG     1117B
CCOMN   MVI     A,125B
        CALL    OUTP
        MVI     A,275B
        CALL    OUTP
        CALL    INP
        CALL    OUTP
        MOV     B,A
        MVI     A,311B
        CALL    OUTP
        MVI     A,275B
        CALL    OUTP
```

```
        CALL    INP
        CALL    OUTP
        MOV     C,A
        CALL    LFCR
        RET
GAINS:  XRA     A
        STA     BB
        MOV     A,B
        CPI     61B
        JZ      VS1
        CPI     62B
        JZ      VS2
        CPI     63B
        JZ      CS1
        CALL    COMND
        JMP     GAINS
VS1:    MVI     A,1
        STA     BB
        JMP     CS1
VS2     MVI     A,2
        STA     BB
CS1     MOV     A,C
        CPI     61B
        JNZ     CS2
        LDA     BB
        ORI     4
        STA     BB
        OUT     377B
        RET
CS2:    CPI     62B
        JNZ     CS3
        LDA     BB
```

```
        ORI     10B
        STA     BB
        OUT     377B
        RET
CS3 :   CPI     63B
        JZ      SETE
        CALL    COMND
        JMP     GAINS
 SETE:  LDA     BB
        ORI     20B
        OUT     377B
        RET
BB :    DB      0
PRINI:  MVI     B,57B
        LXI     H,TWO
        MVI     A,55B
ONE :   CALL    OUTP
        DCR     B
        JNZ     ONE
        CALL    LFCR
        MVI     B,55B
THERE:  MOV     A,M
        CALL    OUTP
        DCR     B
        INX     H
        JNZ     THERE
        CALL    LFCR
        MVI     B,55B
FOUR:   CALL    OUTP
        DCR     B
        JNZ     FOUR
        CALL    LFCR
        RET
```

```
TWO  :      DA      V       11      12      13      14    I(AVE)
DACO :      MOV     A,C
            OUT     375B
            CMA
            OUT     376B
            CALL    CACS
            CALL    CNVT
            CALL    ADCSH
            CALL    PRINT
ADCAV :     PUSH    B
            PUSH    H
            MVI     A,4
            STA     AR
ARA  :      CALL    ADCIN
            XCHG
            CALL    ADCSH
            LXI     B,2000B
TL   :      DCX     B
            MOV     A,B
            ORA     C
            JNZ     TL
            CALL    ADCIN
            DAD     D
            CALL    DIV2
            XCHG
            LHLD    AN
            INX     H
JJ   :      CALL    CNVT
            CALL    ADCSH
            CALL    PRINT
            LDA     AR
            DCR     A
            STA     AR
```

```
        JNZ     ARA
DIV4 :  LHLD    AN
        DCX     H
        MOV     E,M
        DCX     H
        MOV     D,M
        DCX     H
        MOV     C,M
        DCX     H
        MOV     B,M
        DCX     H
        SHLD    AN
        XCHG
        DAD     B
        MVI     A,2
        STA     NAN
NAL  :  XCHG
        LDLD    AN
        MOV     C,M
        DCX     H
        MOV     B,M
        DCX     H
        SHLD    AN
        XCHG
        DAD     B
        LDA     NAN
        DCR     A
        STA     NAN
        JNZ     NAL
        CALL    DIV2
        CALL    DIV2
        XCHG
        CALL    ASAVE
        CALL    CNVT
```

```
        CALL    PRINT
        LXI     H,3000B
        SHLD    AN
        POP     H
        POP     B
        RET
DIV2:   XRA     A
        MOV     A,H
        RAR
        MOV     H,A
        MOV     A,L
        RAR
        MOV     L,A
        RET
ASAVE:  PUSH    H
        LHLD    ARAM
        MOV     M,D
        INX     H
        MOV     M,E
        INX     H
        SHLD    ARAM
        POP     H
        RET
DACS:   PUSH    H
        LHLD    TV
        MOV     M,B
        INX     H
        MOV     M,C
        INX     H
        SHLD    TV
        POP     H
        RET
```

```
AN  :       DW      3000B
AR  :       DB      10B
NAN :       DB      0
ARAM:       DW      3500B
TV  :       DW      4000B
CNVT:       PUSH    H
            PUSH    B
            CALL    ADJST
            MVI     A,14B
            STA     BCD
            LXI     H,ABCD
            LXI     B,0
HAI :       MOV     A,E
            RLC
            MOV     E,A
            MOV     A,D
            RAL
            MOV     D,A
            JNC     CON
            MOV     A,C
            ADD     M
            DAA
            MOV     C,A
            MOV     A,B
            INX     H
            ADC     M
            DAA
            MOV     B,A
            JMP     CONT
CON :       INX     H
CONT:       INX     H
            LDA     BCD
```

```
                DCR         A
                STA         BCD
                JZ          OVER
                JMP         HAI
OVER :          MOV         H,B
                MOV         L,C
                POP         B
                XCHG
                POP         H
                RET
BCD :           DB          14B
 ABCD :         DB 0, 120B,0,45B,120B,22B,45B,6,22B,3,126B,1,170B,
                0,71B,0,31B
BBCD :          DB          0,11B,0,5,0,2,0
ADJST :         PUSH        B
                MVI         B,4
MOVE :          MOV         A,E
                RLC
                MOV         E,A
                MOV         A,D
                RAL
                MOV         D,A
                DCR         B
                JNZ         MOVE
                POP         B
                RET
 PRINT :        MOV         A,D
                CALL        RSFT
                CALL        CUTP
                MOV         A,D
                ANI         17B
                ADI         60B
                CALL        OUTP
```

```
        MOV     A,E
        CALL    RSFT
        CALL    OUTP
        MOV     A,E
        ANI     17B
        ADI     60B
        CALL    OUTP
        MVI     A,240B
        CALL    OUTP
        CALL    OUTP
        CALL    OUTP
        CALL    OUTP
        LDA     LF
        INR     A
        CPI     6
        JZ      LL
        STA     LF
        RET
LL:     XRA     A
        STA     LF
        CALL    LFCR
        RET
LF:     DB      0
ADCIN:  IN      371B
        MOV     E,A
        IN      372B
        ANI     017B
        MOV     D,A
        RET
ADCSH:  MVI     A,7
        OUT     373B
        MVI     A,77B
```

```
DECR :      DCR     A
            JNZ     DECR
            OUT     373B
            RET
RSFT :      RRC
            RRC
            RRC
            ANI     17B
            ADI     60B
            RET
ACHEK :     MOV     A,D
            ORA     E
            RET
PAT :       PUSH    B
            PUSH    D
            PUSH    H
            LHLD    ARAM
            DCX     H
            MOV     E,M
            DCX     H
            MOV     D,M
            DCX     H
            MOV     C,M
            DCX     H
            MOV     B,M
            XCHG
            MOV     D,B
            MOV     E,C
            MOV     A,D
            CMP     H
            JC      SUBT
            JNZ     EXCH
FCHEK :     MOV     A,E
```

```
                CMP     L
                JC      SUBT
                JZ      SUBT
EXCH:           XCHG
 SUBT:          XRA     A
                MOV     A,L
                SBB     E
                MOV     C,A
                MOV     A,H
                SBB     D
                MOV     B,A
                MVI     A,4
                CMP     C
                JC      CLEAR
                STC
                JMP     POPS
 CLEAR:         XRA     A
 POPS:          POP     H
                POP     D
                POP     B
                RET
 DACC:          MOV     A,B
                ORA     C
                RET
 OUTP:          PUSH    PSW
 CHEK:          IN      12B
                RAL
                JNC     CHEK
                POP     PSW
                OUT     13B
                RET
```

```
IMP :       MVI     A,1
            OUT     10B
NN :        IN      10B
            RAL
            JNC     NN
            IN      11B
            ANI     177B
            RET
JK :        MOV     M,E
            INX     H
            SHLD    AN
            JMP     JJ
            END
```